Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.016”**

**.021”**

**D**

**S**

**UP5508**

 **C**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size = .004 x .004”**

**Backside Potential: GATE**

**Mask Ref: UP5508 C**

**APPROVED BY: DK DIE SIZE .016” X .021” DATE: 6/3/19**

**MFG: CALOGIC THICKNESS .010” P/N: J270**

**DG 10.1.2**

#### Rev B, 7/1